WE CLAIM:

1. A method of transferring at least two data streams in a medical device, comprising:

collecting first data stream data into a first intermediate register;

collecting additional data stream data into at least one additional intermediate register; and

storing first intermediate register contents in a first output register.

2. The method of claim 1, further comprising:

storing additional intermediate register contents in the first output register.

3. The method of claim 1, further comprising:

storing first intermediate register contents in at least one additional output register.

4. The method of claim 3 further comprising:

storing remaining first intermediate register contents in the first intermediate register if the additional output register is full.

5. The method of claim 1 further comprising:

storing additional intermediate register contents in at least one additional output register.

6. The method of claim 5 further comprising:

storing remaining additional intermediate register contents in the additional intermediate register if the additional output register is full.

7. The method of claim 1 further comprising:

storing first intermediate register contents with an identification code that uniquely identifies the first data stream data.

8. The method of claim 1 further comprising:

storing additional intermediate register contents with an identification code that uniquely identifies the additional data stream data.

9. The method of claim 1 further comprising:

transferring contents of the first output register to memory.

10. The method of claim 9 further comprising:

transferring contents of an additional output register to memory.

11. The method of claim 1 further comprising:

receiving compressed first data stream data.

12. The method of claim 1 further comprising:

receiving compressed additional data stream data.

13. The method of claim 1 further comprising:

collecting first data stream data until the first intermediate register is full.

14. The method of claim 1 further comprising:

collecting additional data stream data until the additional intermediate register is full.

15. The method of claim 1 further comprising:

storing remaining first intermediate register contents in the first intermediate register if the first output register is full.

16. The method of claim 1 further comprising:

storing remaining additional intermediate register contents in the additional intermediate register if the first output register is full.

17. The method of claim 1 further comprising:

determining a state of the first output register.

18. The method of claim 17 wherein the first intermediate register is full, further comprising:

storing first intermediate register contents in the first output register if the state of the first output register is empty.

19. The method of claim 18 further comprising:

storing first intermediate register contents in the additional output register if the state of the first output register is full.

20. The method of claim 17 wherein the additional intermediate register is full, further comprising:

storing additional intermediate register contents in the first output register if the state of the first output register is empty.

21. The method of claim 20 further comprising:

storing additional intermediate register contents in the additional output register if the state of the first output register is full.

22. A medical device comprising:

a processor;

a controller operably connected to the processor;

at least one sensor operably connected to the controller for collecting data, wherein the data comprises data from a first data stream and at least one additional data stream;

a memory transfer unit for transferring the data to a memory;

a first intermediate register for collecting first data stream data;

at least one additional intermediate register for collecting additional data stream data; and

at least one output register for receiving first intermediate register contents.

23. The device of claim 22, further comprising:

an additional output register for receiving first intermediate register contents.

24. The device of claim 22, further comprising:

an additional output register for receiving additional intermediate register contents.

25. The device of claim 22 wherein the output register receives additional intermediate register contents.

26. The device of claim 22 further comprising:

a memory operably connected to the processor for storing the data.

27. The device of claim 22 wherein the first intermediate register contents include an identification code that uniquely identifies the first intermediate register contents.

28. The device of claim 22 wherein the additional intermediate register contents include an identification code that uniquely identifies the additional intermediate register contents.

29. The device of claim 22 wherein the first intermediate register is adapted to store first data stream data.

30. The device of claim 22 wherein the additional intermediate register is adapted to store additional data stream data.

31. The device of claim 22 further comprising:

a converter operably connected to the processor for converting at least one signal to the data.

32. A system for transferring at least two data streams in a medical device, comprising:

means for collecting first data stream data into a first intermediate register;

means for collecting additional data stream data into at least one additional intermediate register; and

means for storing first intermediate register contents in a first output register.

33. The system of claim 32, further comprising:

means for storing additional intermediate register contents in the first output register.

34. The system of claim 32, further comprising:

means for storing first intermediate register contents in at least one additional output register.

35. The system of claim 34, further comprising:

means for storing remaining first intermediate register contents in the first intermediate register if the additional output register is full.

36. The system of claim 32, further comprising:

means for storing additional intermediate register contents in at least one additional output register.

37. The system of claim 36, further comprising:

means for storing remaining additional intermediate register contents in the additional intermediate register if the additional output register is full.

38. The system of claim 32, further comprising:

means for storing first intermediate register contents with an identification code that uniquely identifies the first data stream data.

39. The system of claim 32, further comprising:

means for storing additional intermediate register contents with an identification code that uniquely identifies the additional data stream data.

40. The system of claim 32, further comprising:

means for transferring contents of the first output register to memory.

41. The system of claim 40, further comprising:

means for transferring contents of an additional output register to memory.

42. The system of claim 32, further comprising:

means for collecting first data stream data until the first intermediate register is full.

43. The system of claim 32, further comprising:

means for collecting additional data stream data until the additional intermediate register is full.

44. The system of claim 32, further comprising:

means for storing remaining first intermediate register contents in the first intermediate register if the first output register is full.

45. The system of claim 32, further comprising:

means for storing remaining additional intermediate register contents in the additional intermediate register if the first output register is full.

46. The system of claim 32, further comprising:

means for determining a state of the first output register.

47. A computer usable medium including a program for transferring data in an implantable device, comprising:

computer program code that collects first data stream data into a first intermediate register;

computer program code that collects additional data stream data into at least one additional intermediate register; and

computer program code that stores first intermediate register contents in a first output register.

48. The program of claim 47, further comprising:

computer program code that stores additional intermediate register contents in the first output register.

49. The program of claim 47, further comprising:

computer program code that stores first intermediate register contents in at least one additional output register.

50. The program of claim 49 further comprising:

computer program code that stores remaining first intermediate register contents in the first intermediate register if the additional output register is full.

51. The program of claim 47 further comprising:

computer program code that stores additional intermediate register contents in at least one additional output register.

52. The program of claim 51 further comprising:

computer program code that stores remaining additional intermediate register contents in the additional intermediate register if the additional output register is full.

53. The program of claim 47 further comprising:

computer program code that stores first intermediate register contents with an identification code that uniquely identifies the first data stream data.

54. The program of claim 47 further comprising:

computer program code that stores additional intermediate register contents with an identification code that uniquely identifies the additional data stream data.

55. The program of claim 47 further comprising:

computer program code that transfers contents of the first output register to memory.

56. The program of claim 55 further comprising:

computer program code that transfers contents of an additional output register to memory.

57. The program of claim 47 further comprising:

computer program code that receives compressed first data stream data.

58. The program of claim 47 further comprising:

computer program code that receives compressed additional data stream data.

59. The program of claim 47 further comprising:

computer program code that collects first data stream data until the first intermediate register is full.

60. The program of claim 47 further comprising:

computer program code that collects additional data stream data until the additional intermediate register is full.

61. The program of claim 47 further comprising:

computer program code that stores remaining first intermediate register contents in the first intermediate register if the first output register is full.

62. The program of claim 47 further comprising:

computer program code that stores remaining additional intermediate register contents in the additional intermediate register if the first output register is full.

63. The program of claim 47 further comprising:

computer program code that determines a state of the first output register.

64. The program of claim 63 wherein the first intermediate register is full, further comprising:

computer program code that stores first intermediate register contents in the first output register if the state of the first output register is empty.

65. The program of claim 64 further comprising:

computer program code that stores first intermediate register contents in the additional output register if the state of the first output register is full.

66. The program of claim 63 wherein the additional intermediate register is full, further comprising:

computer program code that stores additional intermediate register contents in the first output register if the state of the first output register is empty.

67. The program of claim 66 further comprising:

computer program code that stores additional intermediate register contents in the additional output register if the state of the first output register is full.